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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/809,337	03/26/2004	Keiichi Kushida	250793US2SDIV	8237

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EXAMINER	
LE, VU ANH	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 01/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/809,337	KUSHIDA, KEIICHI	
	Examiner	Art Unit	
	Vu A. Le	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *14-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *14-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 November 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/419174.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

1. Claims 17-18 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

2. The newly added claims 17-18 recite "at least one selection circuit which applies second voltage VSS - ΔV, which is lower than a first voltage VSS, to the source terminal of the N-type MOS transistor of the second CMOS inverter circuit of the 5-transistor cells through said at least one VSS power line in "1" data write mode, or applies the first voltage VSS to the source terminal of the N-type MOS transistor of the second CMOS inverter circuit of the 5-transistor cells through said at least one VSS power line in another mode." This feature raises a new matter which is not supported in the specification.

Response to Amendment

3. The amendment filed 11/18/04 is objected to under 35 U.S.C. 132 because it introduces new matter into the disclosure. 35 U.S.C. 132 states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows: The original specification supports the second voltage **VSS+ΔV** as depicted in Figures 8 and 9 for the third and fourth embodiments. The newly added material the second voltage **VSS-ΔV** in new claims 17-18 with newly corrected Figure 8 and specification (to explain Figure 8) raises new matter. It is not an obvious error since this change is added in the present amendment for Figure 8 (the third embodiment) only. The fourth embodiment, Figure 9, still use second voltage **VSS+ΔV** and the amended claim 14 still recite the second voltage **VSS+ΔV** (see further explanation in the Response to Arguments section below).

Applicant is required to cancel the new matter in the reply to this Office Action.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lattimore et al (5,831,896) in view of Rapp (4,189,785).

6. Lattimore et al disclose a five transistor memory cell device having all the claimed features such as 5 transistor SRAM, pass gate transistor connected between bit line and the output of the first inverter, a selection circuit, etc. Lattimore et al fails to disclose a voltage of **VSS+ΔV** is connected to memory cell in writing data "1" mode. However, Rapp (Fig.3) teaches a voltage of **VSS+ΔV** is connected to memory cell in writing "1" data mode (a Vguard (2 volts) or a Vzero (1 volt) is applied to memory cell. Therefore, it would have been obvious to one of ordinary skill in the art at the time this invention was made to modify Lattimore et al by connecting the memory to a voltage of **VSS+ΔV** (1 or 2 volts) such as taught by Rapp in order to increase the reliable establishment of cell latching for a wide variation in MOSFET characteristics resulting from manufacturing process (col.4, line 25-27).

Response to Arguments

7. Applicant's arguments filed 11/18/04 have been fully considered but they are not persuasive.

8. The applicant argues that an obvious error has been made. For example, applicant states "M.P.E.P. 2163.07 indicates that an amendment to correct an obvious error does not constitute new matter where one skilled in the art would not only recognize the existence of the error in the specification, but also the appropriate correction. In the present case, Applicant submits that the designation of the applied voltage **V+ΔV** ***in Figure 8*** as originally filed and the associated discussion with regard to ***Figure 8 of*** **V+ΔV** in the specification was an obvious error, and that one skilled in the

art would both recognize the existence of this error and the appropriate correction thereof" and "Thus, one of ordinary skill in the art would not only recognize that **VSS+ΔV** is erroneous" because the first and second embodiments of the present invention and in the corresponding Figures 1 and 3, the applied voltage is decreased by application of **VDD-ΔV.**

9. This argument is found not persuasive because in the first and second embodiments of the present invention and in the corresponding Figures 1 and 3, the applied voltage is **VDD** ***which is different from the applied voltage*** **VSS** *as recited in the newly added independent claim 17.* In the first and second embodiments of the present invention and in the corresponding Figures 1 and 3, the applied voltage **VDD-ΔV** is applied to the **P-type MOS transistor** while the newly added independent claim 17 recites **VSS-ΔV** being applied to **N-type MOS transistor.** In short, this is not an obvious error since the same concept of reduce voltage can not be applied to **two different kind of transistors** by using **two different kind of voltage sources**.

10. Furthermore, the applicant seems to contradict to himself when the newly amended claim 14 recites second voltage **VSS+ΔV** while the newly added claim 17 recites second voltage **VSS-ΔV.** If the second voltage **VSS+ΔV** is an obvious error why it still keep unchanged in the newly amended claim 14.

11. Another contradiction is **the same** second **VDD-ΔV** is applied to the source of transistor 22a in Fig.1 and to the sources of transistors 21a and 22a in Fig.3 but second voltage **VSS+ΔV** is applied to the source of transistor 21b in Fig.8 (as recited in claim

14) while **another** second voltage **VSS-ΔV** is applied to the sources of transistors 21b and 22b in Fig.9 (as recited in claim 17).

12. The applicant argues that the newly amended claim 14 recites the second voltage **VSS+ΔV** is applied in writing "1" data mode and the first voltage Vss is applied in another mode. This argument is found not persuasive since Rapp, Figure 3, teach the Vss is applied in another mode too.

13. The applicant argues that the Rapp's structure presenting practical noise problems. However, in 103 rejection, the Lattimore's structure is combined with the use of Vguard or Vzero of Rapp. Therefore, this argument is found not persuasive.

Conclusion

14. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vu A. Le whose telephone number is (571) 272-1871. The examiner can normally be reached on M-F (7:00-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vu A. Le
Primary Examiner
Art Unit 2824

01/05/05